CLAIMS

What is claimed is:

1. A receiver equalizer, comprising:

samplers for sampling an incoming input data stream according to plural phases of a sampling clock, each sampler producing a data sample; and

a multi-tap finite impulse response (FIR) filter which, in an analog domain, for each data sample, weights said data sample and at least one previous data sample, and combines said weighted data samples to produce an equalized data bit.

2. The equalizer of Claim 1, wherein the multi-tap FIR comprises:

a first current source that produces a first current which is proportional to a product of a previous data sample and a weight associated with said previous data sample tap;

a second current source that produces a second current which is proportional to an instance data sample;

an adder circuit which subtracts the second current from the first current to produce a third current; and

a converter circuit which converts the third current to a voltage corresponding to the equalized data bit.

3. The equalizer of Claim 1, wherein the equalizer compensates for characteristics of a communications channel.

4. The equalizer of Claim 3, wherein the communications channel is a multi-gigabit per second link.

5. The equalizer of Claim 3, wherein the communications channel is a cable.

6. The equalizer of Claim 3, wherein the communications channel is a circuit board trace.

7. The equalizer of Claim 3, wherein the communications channel is an optical fiber.

8. The equalizer of Claim 3, wherein the communications channel has low-pass characteristics.

9. The equalizer of Claim 1, wherein the FIR filter is a high-pass filter.

10. The equalizer of Claim 1, further comprising:

second samplers for sampling and holding the equalized data bit values; and

sense amplifiers for converting the sampled equalized data bit values to digital values.

11. A method for equalizing an incoming input data stream, comprising:

sampling the input data stream according to plural phases of a sampling clock to produce data samples; and

filtering the data samples with an analog multi-tap finite impulse response (FIR) filter to produce equalized data bits.

12. The method of Claim 11, wherein filtering comprises:

in an analog domain, weighting the data samples; and

combining the weighted data samples to produce an equalized data bit.

13. The method of Claim 12, wherein the FIR filter is a high-pass filter.

14. The method of Claim 11, further comprising:

sampling and holding the equalized data bit values; and

converting the sampled equalized data bit values to digital values.

15. A receiver equalizer, comprising:

means for sampling the input data stream according to plural phases of a sampling clock to produce data samples; and

means for filtering the data samples with an analog multi-tap finite impulse response (FIR) filter to produce equalized data bits;

means for sampling and holding the equalized data bit values; and

means for converting the sampled equalized data bit values to digital values.

16. A multi-tap analog finite impulse response filter, comprising:

a first current source that produces a first current which is proportional to a product of a previous data sample and a weight associated with said previous data sample tap; and

a second current source that produces a second current which is proportional to an instance data sample;

an adder circuit which subtracts the second current from the first current to produce a third current; and

a converter circuit which converts the third current to a voltage corresponding to the equalized data bit.

17. A multi-tap analog finite impulse response filter method, comprising:

producing a first current which is proportional to a product of a previous data sample and a weight associated with said previous data sample tap;

producing a second current which is proportional to an instance data sample;

subtracting the second current from the first current to produce a third current; and

converting the third current to a voltage corresponding to the filtered data bit.

18. A multi-tap analog finite impulse response filter, comprising:

means for producing a first current which is proportional to a product of a previous data sample and a weight associated with said previous data sample tap;

means for producing a second current which is proportional to an instance data sample;

means for subtracting the second current from the first current to produce a third current; and

means for converting the third current to a voltage corresponding to the filtered data bit.